Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

70. (previously presented) A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of aid memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices; and

test mode logic for determining whether the memory is in a test mode, and wherein said plurality of peripheral devices includes a latching circuit responsive to a first external signal when the memory is in the test mode, for latching data stored in a first seed group of memory elements, and an enable circuit responsive to a second external signal when said memory is in the test mode, for enabling the latched data to be written to a second group of memory elements.

71. (previously presented) A method of testing a plurality of memory elements organized in a plurality of rows, comprising the steps of:

writing test data into a first seed row of memory elements;

latching the test data from the first seed row of memory elements in response to a first external signal;

writing the latched test data into subsequent groups of memory elements in response to a second external signal;

reading the test data from the subsequent groups of memory elements; and

comparing the test data read from the subsequent groups of memory elements with the test data written to the first seed row of memory elements.

100. (previously presented) A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising: an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral device; and

test mode logic for determining whether the memory is in a test mode, and wherein said plurality of peripheral devices includes a latching circuit responsive to a first external signal when the memory is in the test mode, for latching data stored in a first seed group of memory cells, and an enable circuit responsive to a second external signal when said memory is in the test mode, for enabling the latched data to be written to a second group of memory cells.

120. (previously presented) A combination for use in a memory having an array of memory elements, said combination comprising:

test mode logic for determining whether the memory is in a test mode;

a latching circuit responsive to a first external signal when the memory is in the test mode, for latching data stored in a first group of memory elements; and

an enable circuit responsive to a second external signal when the memory is in the test mode, for enabling the latched data to be written to a second group of memory elements.

126. Cancelled

135. (previously presented) A method of testing a portion of a memory array having a plurality of memory elements formed in a plurality of rows, and wherein said array is arranged in a plurality of memory blocks, said method comprising the steps of:

selecting a memory block for testing:

writing test data into a first seed row of memory elements in the selected memory block;

latching the test data from the first seed row of memory elements in response to a first external signal;

writing the latched test data into subsequent pluralities of rows of memory elements in response to a second external signal;

reading the test data from the memory block; and

comparing the test data read from the memory block with the test data written into the first seed row.

136. (previously presented) The method of claim 135 wherein the first external signal is a row address strobe signal and the second external signal is a column address strobe signal.

138. – 142. Cancelled

143. (previously presented) A method of inputting test mode information to a solid state device, comprising:

enabling a detector;

inputting to the device a voltage outside the range of voltages used to represent logic signals;

confirming the presence of the voltage outside the range of voltages used to represent logic signals; and

inputting to the device at least one address containing test mode information.

147. (previously presented) A method of placing a solid state device into a test mode, comprising:

applying to the device a voltage outside the range of voltages used to represent logic signals, and while said voltage is being applied;

sequentially inputting at least two addresses to said device, said first address containing information used to confirm the presence of said voltage outside the range of voltages used to represent logic signals, and said second address containing information used to place the device into a test mode.

152. (previously presented) A method of placing a solid state memory device into a test mode, comprising:

applying to the device a voltage outside the range of voltages used to represent logic signals, and while said voltage is being applied;

applying a specific combination of control signals to enable the receipt of a test enable key;

verifying the test enable key and confirming the presence of the applied voltage;

applying said specific combination of control signals to enable the receipt of at least one test mode key; and

decoding the test mode key to place the device in a test mode.

160. (previously presented) A test logic circuit for a solid state memory device, comprising:

a test mode enable circuit for determining if a voltage outside the range of voltages used to represent logic levels is being applied to the memory device under predetermined conditions; and

a circuit for receiving and decoding test mode keys in response to said test mode enable circuit.

161. (previously presented) The test logic circuit of claim 160 additionally comprising a test mode reset circuit for resetting said circuit for receiving and decoding test mode keys.

162. (previously presented) The test logic circuit of claim 160 additionally comprising a circuit for inhibiting said solid state memory device from normal operations when the device is in a test mode.

163. (previously presented) A solid state memory device, comprising:

a plurality of memory cells;

a plurality of peripheral devices for writing information into and reading information out of said memory cells; and

a test logic circuit, comprising:

a test mode enable circuit for determining if a voltage outside the range of voltages used to represent logic levels is being applied to the memory device under predetermined conditions; and

a circuit for receiving and decoding test mode keys in response to said test mode enable circuit;

said memory device further comprising circuits, responsive to said decoded test mode keys, for performing tests on at least one of said memory cells and peripheral devices.

164. (previously presented) The memory device of claim 163 wherein said test mode enable circuit includes logic for receiving a row address strobe signal (RAS), a write column address strobe before RAS signal, the applied voltage, and certain address information on column address lines and for producing therefrom a latch signal.

165. (previously presented) The memory device of claim 164 additionally comprising a test mode reset circuit for resetting said circuit for receiving and decoding test mode keys.

166. Cancelled

167. (previously presented) The memory of claim 70 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

168. (previously presented) The memory of claim 167 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

169. (previously presented) The memory of claim 70 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

170. (previously presented) The memory of claim 70 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

171. (previously presented) The memory of claim 70 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

172. (previously presented) The memory of claim 70 wherein said memory provides at least 256 meg of storage.

173. (previously presented) The memory of claim 172 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

174. (previously presented) The method of claim 71 wherein the first external signal is a row address strobe signal and the second external signal is a column address strobe signal.

175. (previously presented) The method of claim 174 wherein writing into subsequent groups of memory elements includes writing into multiple rows in response to each cycle of the column address strobe signal.

176. (previously presented) The system of claim 100 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

177. (previously presented) The system of claim 176 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

178. (previously presented) The system of claim 100 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

179. (previously presented) The system of claim 178 additionally comprising a plurality of pads located centrally with respect to said array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

180. (previously presented) The system of claim 179 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

181. (previously presented) The system of claim 180 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

182. (previously presented) The system of claim 180 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate or concurrent operation to achieve a predetermined level of output power.

183. (previously presented) The system of claim 100 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

184. (previously presented) The system of claim 100 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

185. (previously presented) The system of claim 100 wherein said memory provides at least 256 meg of storage.

186. (previously presented) The system of claim 185 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

187. (previously presented) The combination of claim 120 wherein said first external signal includes a row address strobe signal.

188. (previously presented) The combination of claim 120 wherein said second external signal includes a column address strobe signal.

189. – 195. Cancelled

196. (previously presented) The method of claim 143 wherein said step of enabling a detector is performed by the step of inputting a sequence of control signals.

197. (previously presented) The method of claim 196 wherein said sequence of control signals includes a write enable signal, column address strobe signal and row address strobe signal.

198. (previously presented) The method of claim 143 wherein said step of inputting at least one address to the device is performed while said step of inputting a voltage is performed.

199. (previously presented) The method of claim 143 wherein said step of inputting at least one address includes the step of inputting a first address for confirming that the device is to be in a test mode and inputting a second address for specifying a test mode.

200. (previously presented) The method of claim 147 additionally comprising the step of inhibiting the device from normal operation while said step of applying a voltage is performed.

201. (previously presented) The method of claim 147 additionally comprising the step of ending the application of a voltage outside the range of voltages used to represent logic signals to take the device out of a test mode.

202. (previously presented) The method of claim 147 additionally comprising the step of inputting an address containing information to take the device out of a test mode.

203. (previously presented) The method of claim 152 wherein the step of applying a voltage includes the step of applying a voltage higher than the highest voltage used to represent logic signals in the device.

204. (previously presented) The method of claim 152 additionally comprising the step of inhibiting the device from normal operation while said step of applying a voltage is performed.

205. (previously presented) The method of claim 152 additionally comprising the step of ending the application of a voltage outside the range of voltages used to represent logic signals to take the device out of a test mode.

206. (previously presented) The method of claim 152 additionally comprising the step of inputting a clear test mode key to take the device out of a test mode.

207. (previously presented) The method of claim 152 wherein said test mode keys are received as address information on column address lines.

208. (previously presented) The method of claim 152 additionally comprising the steps of performing the test specified by the test mode key and outputting the test results.